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Attorney's Docket No. 042390.P5832

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application for:

Donald S. Gardner, et al.

Serial No. 09/253,306

Filed: February 19, 1999

For: **INTERCONNECTION ALLOY FOR INTEGRATED CIRCUITS**

Examiner: Tran, T.

Art Unit: 2811

DECLARATION PURSUANT TO 37 C.F.R. § 1.131

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

I, Thomas N. Marieb, hereby declare that:

1. I am a citizen of the United States of America.
2. I currently reside at 1651 11th Avenue, San Francisco, California 94122.
3. I am currently and have been employed by Intel Corporation ("Intel") since 1994.
4. My position at Intel is Principal Engineer.
5. I am a co-inventor of the above-identified patent application.
6. Intel is the assignee of the above-identified patent application.
7. I have reviewed U.S. Patent No. 6,277,730B1 issued to Yuasa (the "Yuasa" patent) which was filed on February 16, 1999. The Examiner has cited the Yuasa patent against the claims of the above-identified application.

8. The invention disclosed and claimed in the above-identified patent application was conceived in the United States of America at least as early as February 16, 1999, as evidenced by the attached document entitled "Intel Invention Disclosure Form." This document was reduced to writing at least as early as February 16, 1999. This document demonstrates conception of the invention of the instant application, and it was prepared based upon my own original work. Between its conception and its constructive reduction to practice by the filing of the above-identified patent application on February 19, 1999, co-inventor Donald S. Gardner and I directed simulations in a diligent effort to reduce the invention to practice. Therefore, the conception and diligence towards reduction to practice of the invention disclosed and claimed in the above-identified patent application occurred prior to the earliest priority date of the Yuasa patent.

9. The document provided herewith is designated "Intel Confidential." It is Intel's practice to maintain in secrecy all documents designated "Intel Confidential." I believe that the document from which these excerpts come has at all times prior to the filing date of the above-captioned application been maintained in a confidential manner.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the above-identified application or any patent issued thereon.

Respectfully submitted,

Dated: 5/16/2002

Thomas N. Marieb

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INTEL CONFIDENTIAL

INTEL INVENTION DISCLOSURE

LEGAL ID# 8861 TMG/CRL DATE: [redacted]

It is important to provide accurate and detailed information on this form. The information will be used to evaluate your invention for possible filing as a patent application. When completed, please return this form to the Legal Department at RN4-01. If you have any questions regarding this form or to whom it should be forwarded, please call [redacted] or [redacted].

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TECHNOLOGY CENTER 2800

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(PROVIDE SAME INFORMATION AS ABOVE FOR EACH ADDITIONAL INVENTOR)

2. Title of Invention Al-Cu-Ti Alloys for Interconnections in Integrated Circuits

3. Stage of development, i.e. % complete, and relation of technology to the following product/process: [redacted]

4. (a) Has a description of your invention been, or will it shortly be, published outside Intel:

NO: X YES: _____ DATE WAS OR WILL BE PUBLISHED: _____

If YES, was the manuscript submitted for pre-publication approval? YES: _____ NO: _____

(b) Has your invention been used/sold or planned to be used/sold by Intel or others?

NO: X YES: _____ DATE WAS OR WILL BE SOLD: _____

5. If invention conceived, or constructed during performance of a government or third party contract, please check here ____ and give the contract name and number _____

6. Please attach a page to this form, DATED AND SIGNED BY ONE INVENTOR (PREPARER), to provide an abstract of your invention, and include the following information in your abstract:

(a) State general purpose(s) of your invention;
(b) Describe advantage(s) of your invention over what is done now;
(c) Describe essential element(s) or key to your invention; and
(d) Value of your invention to Intel (how will it be used?).

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*HAVE YOUR SUPERVISOR READ, DATE AND SIGN COMPLETED FORM. DATABASE DEPT.

DATE: [redacted] SUPERVISOR: [redacted]

BY THIS SIGNING, I (SUPERVISOR) ACKNOWLEDGE THAT I HAVE READ AND UNDERSTAND THIS DISCLOSURE, AND RECOMMEND THAT THE HONORARIUM BE PAID.

[redacted]

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Al-Cu-Ti Alloys for Interconnections in Integrated Circuits

Donald S. Gardner
Thomas A. Marieb

Interconnections increasingly determine the limits in performance, reliability and power consumption for ULSI and require new materials. A technique to improve the interconnection metallization is to alloy aluminum with small amounts of another element such as copper that has a low residual resistivity and solid solubility in aluminum. Al-0.5%Cu is commonly used today in interconnections, but further improvement is needed. A new alloy being considered for interconnections is Al-Cu-Ti because of its minimal impact on resistivity and potentially higher reliability.

Good resistivity can be maintained in aluminum alloys by keeping the solubility low because the lattice of the aluminum matrix is not distorted, instead precipitates form or the solute segregates at the grain boundaries. Precipitates do not have a detrimental effect on the resistivity and can potentially improve the electromigration and stress voiding lifetimes. Measurements of the resistivity of Al-0.5%Cu-0.1%Ti were found to be similar to Al-0.5%Cu with values of 2.8 to 3.1 μΩ-cm. The maximum solid solubility of titanium in pure aluminum is 0.57 at.% and the *residual resistivity* is about 2.9 μΩ-cm per 0.5 at.% titanium [1]. This would result in a higher resistivity than that observed in the Al-Cu-Ti alloys of about 3.5 μΩ-cm when taking into account the 0.81 μΩ-cm/at.% residual resistivity of copper in aluminum[2]. The difference is probably because the copper is acting like silicon does in Al-Si-Ti alloys. When silicon is added with titanium in aluminum, the resistivity of a homogeneous aluminum alloy typically drops by 25 percent [3]. The silicon is reducing the solid solubility of titanium in aluminum and providing a mechanism for the formation of $Ti(Al,Si)_3$ thereby eliminating the supersaturation of titanium in aluminum [3]. The solid solubility is also a function of temperature and becomes negligible at room temperature if the structure were in equilibrium, so the resistivity also depends on the thermal treatment.

In electromigration tests, the addition of 0.1 at.% Ti to the traditional Al-0.5%Cu increased lifetime in single level test structures by a factor of at least two while keeping resistivity about the same. The metallization used in the test were multilayered structures that are similar to those commonly found in microchips today, a Ti/TiN/Al alloy/Ti/TiN.

This electromigration improvement in combination with the minimal impact on resistivity make this alloy a promising new candidate for interconnection metallization.

[1] E. Babic, R. Krsnik, and M. Ocko, J. Physics F: Metal Phys., 6(1), pp. 73-83, 1976.
[2] F. M. d'Heurle and A. Gangulee, in Reliability Physics Symp., IEEE, 10 pp. 165-170, 1972.
[3] D. S. Gardner, Ph.D. Thesis, Stanford Univ, pp. 132-140, 1988.

Read & Understood [redacted]

[redacted]